

MODEL NAME : VBW10
PROJECT CODE : ANRVBW0100
PCB NO : DA8000WM000 LA-9983P M/B
DA40001FP00 LS-9102P USB/B
DA40001FR00 LS-9104P ODD/B
DA40001G400 LS-9105P POWER BUTTON/B
DA40001FQ00 LS-9106P TP BUTTON/B

Dell / Compal Confidential

Schematic Document

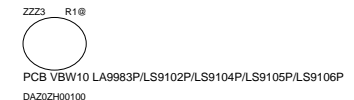
Intel Shark Bay ULT
OAK Value2
UMA/DIS AMD Sun XT

2013-05-29

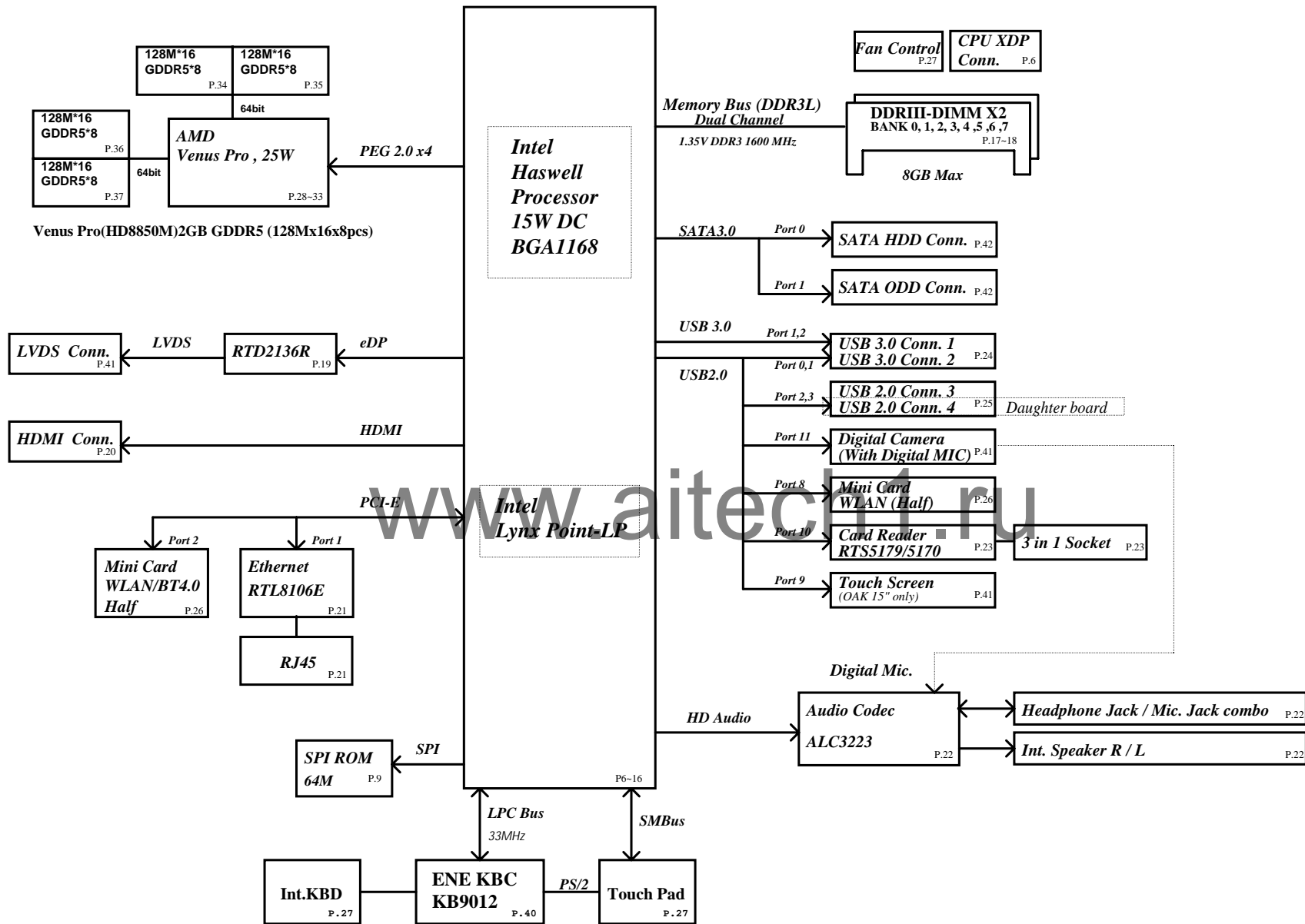
Rev: 1.0

X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
UMA@ : Only for UMA
DIS@ : Only for Discrete
SUN@ : SUN XT
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
RF@ : RF parts
X@ : cost down

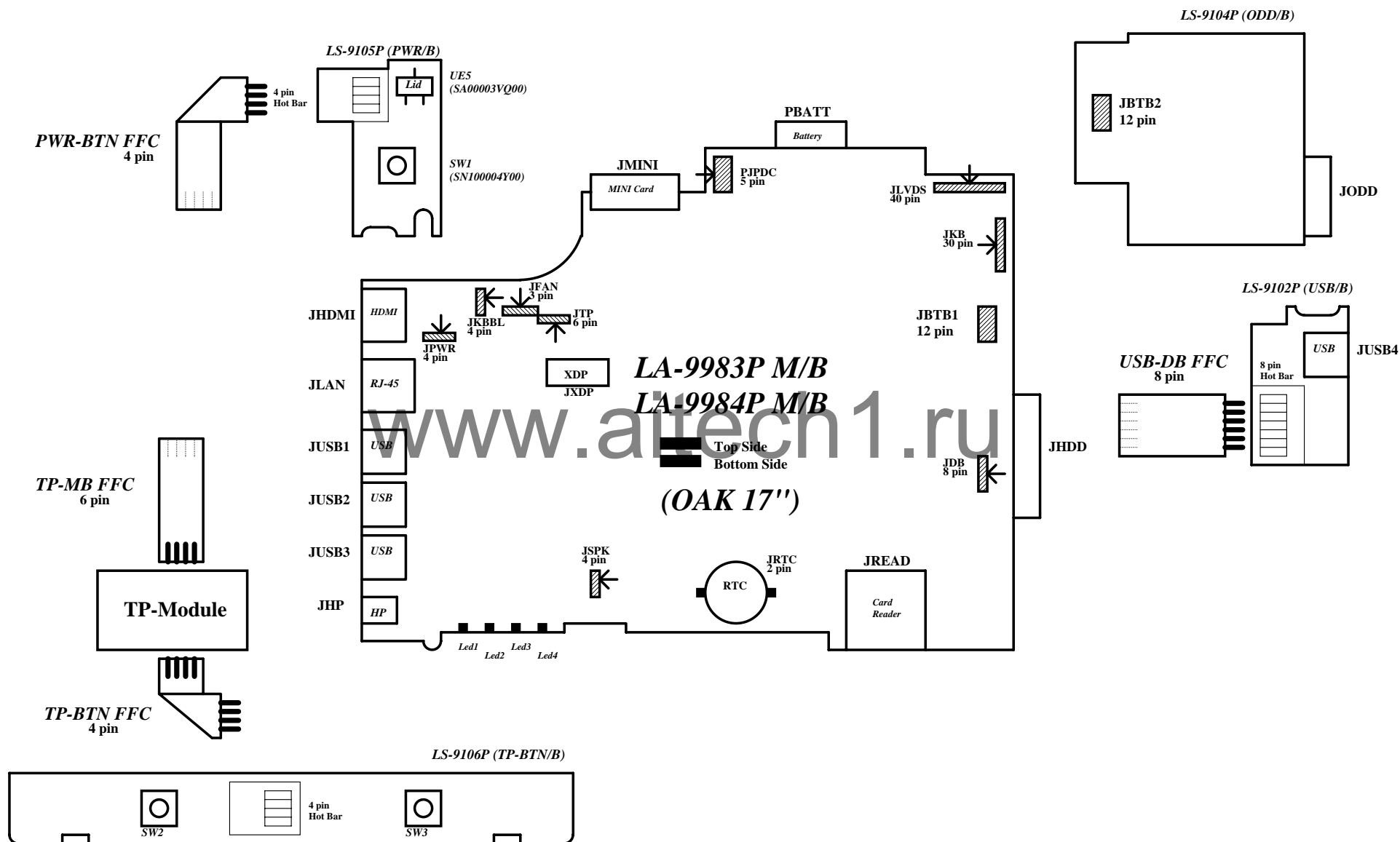
BOM config
UMA : UMA@,EMI@,ESD@,RF@
DIS SUN : SUN@,DIS@,EMI@,ESD@,RF@,X76@



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Project Code : VAW10 / VAW11
File Name : LA-9983P / LA-9984P



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Board ID Table for AD channel

VCC	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF


SMBUS Control Table

	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SML0CLK SML0DATA	ULT								
SML1CLK SML1DATA	ULT								

Board ID TABLE

ID	PCB Revision			
	UMA	Sun XT	VenusPro	VenusXT
0	SSI&A02			
1		SSI&A02		
2			SSI&A02	
3				SSI&A02
4	PT			
5		PT		
6			PT	
7				PT
8	ST			
9		ST		
10			ST	
11				ST
12	XB			
13		XB		
14			XB	
15				XB
16	A01			
17		A01		
18			A01	
19				A01

Symbol Note :

 : means Digital Ground

 : means Analog Ground

CLOCK SIGNAL

CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

ULT

Link

USB3.0

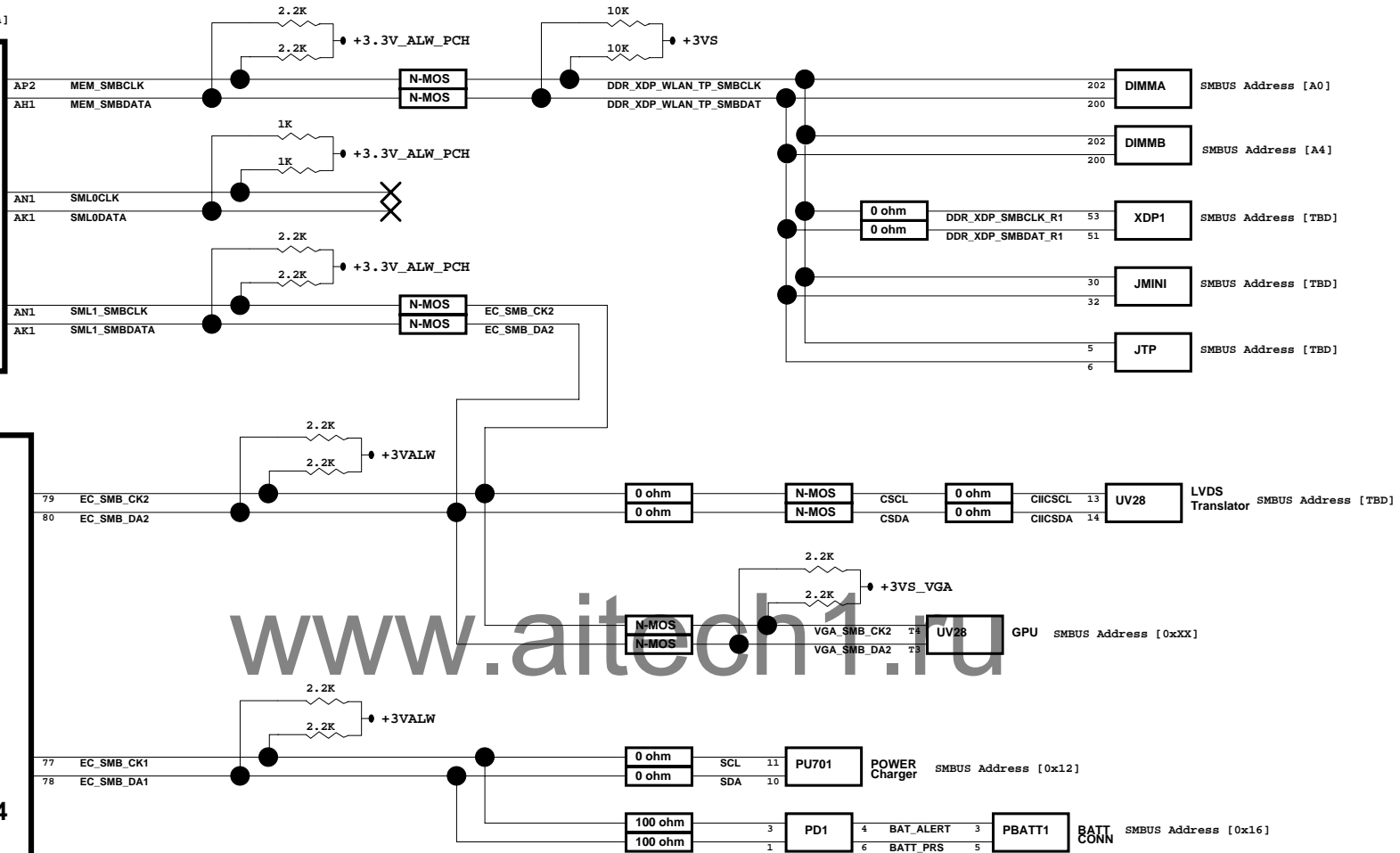
Port1	USB connector 2
Port2	USB connector 1
Port3	
Port4	
USB2.0	
Port0	USB connector 2
Port1	USB connector 1
Port2	USB connector 3
Port3	USB connector 4 (DB)
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (N14P)
Lane 6	PEG (N14P)
SATA	
SATA0	HDD
SATA1	ODD
SATA2	
SATA3	

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SMBUS Address [0x9a]

MCH
Shark bay

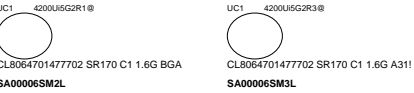
KBC
KB9012A4



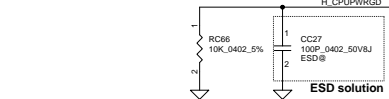
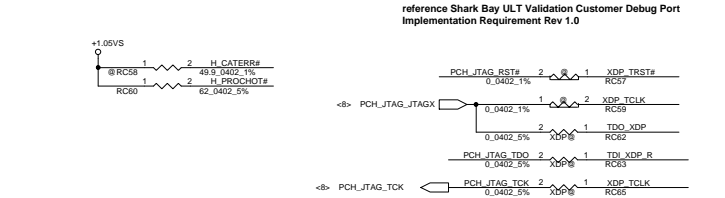
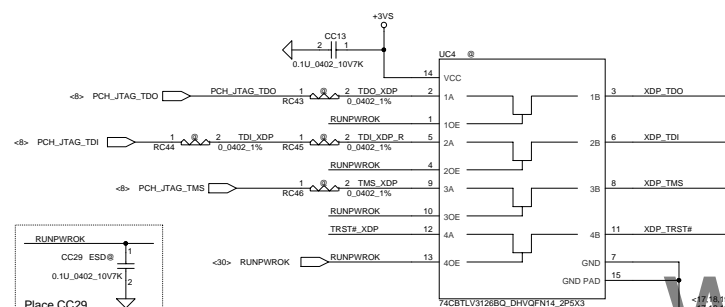
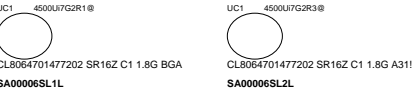
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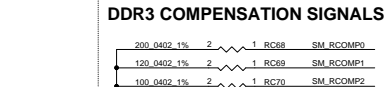
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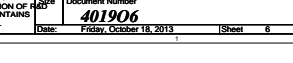
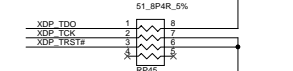
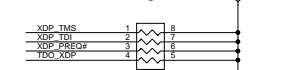
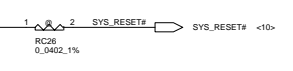
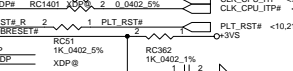
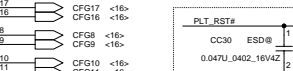
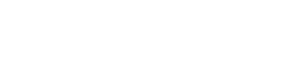
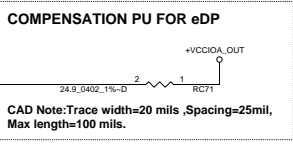
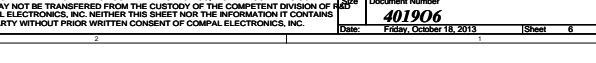
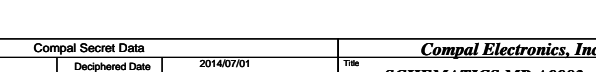
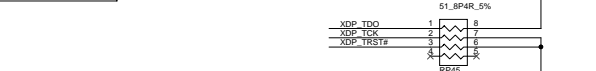
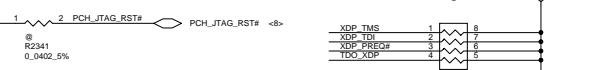
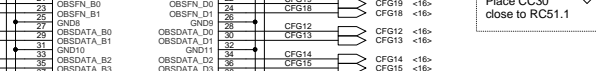
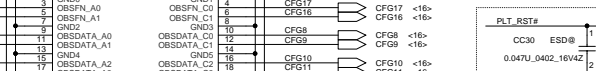
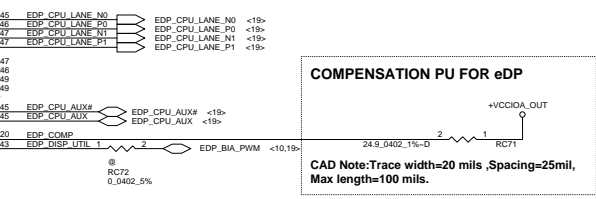
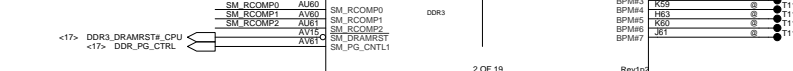
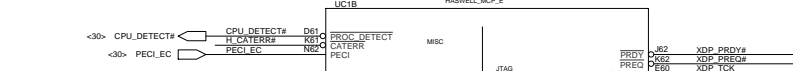
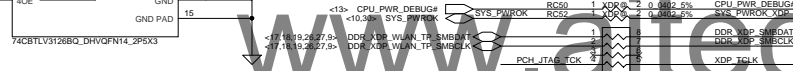
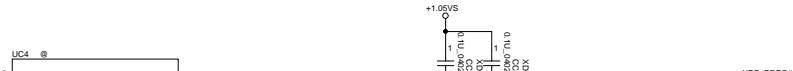
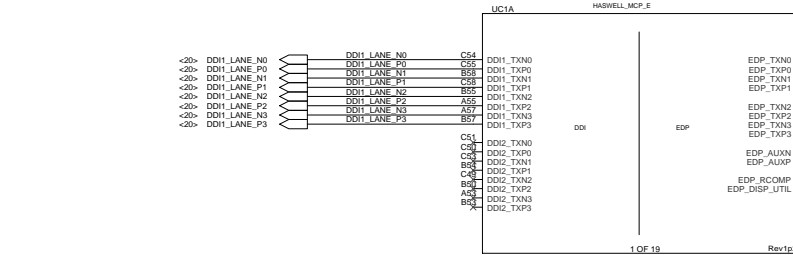
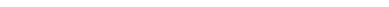
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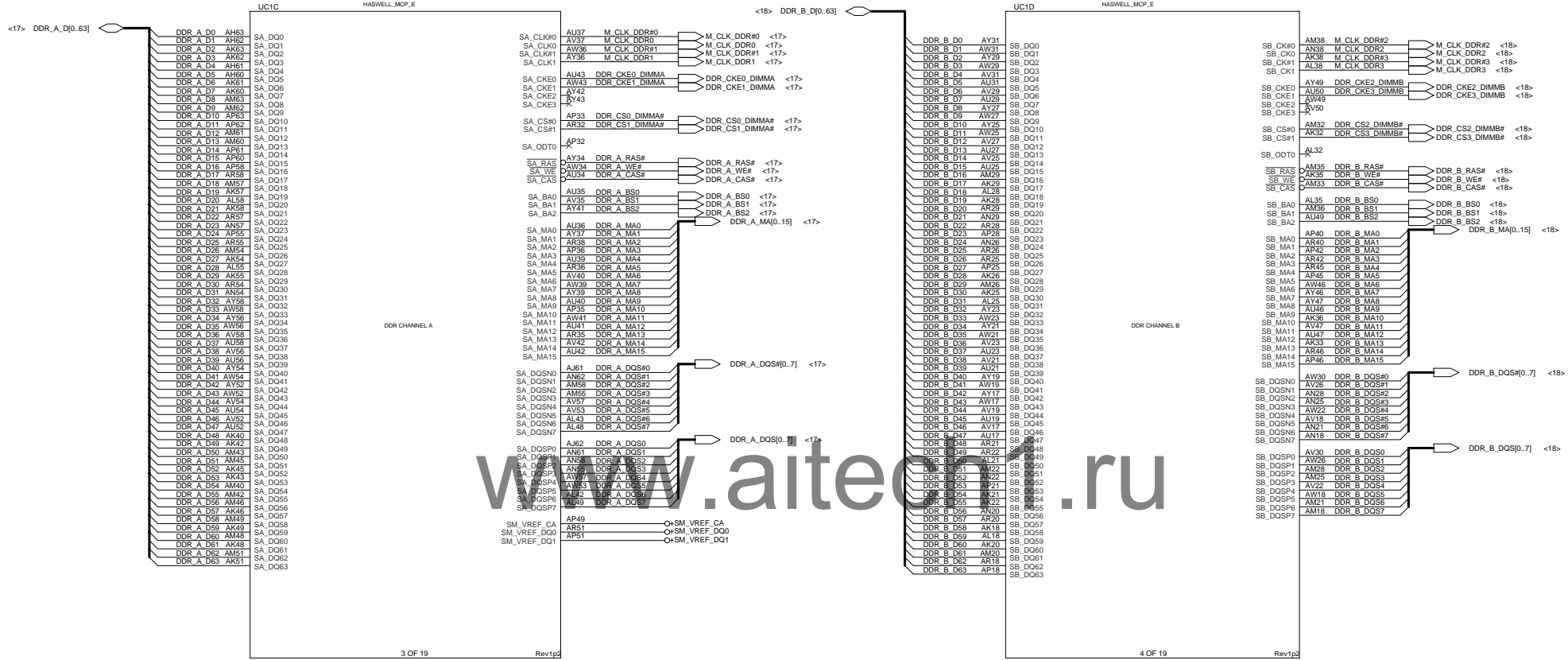
CAD Note:
Avoid stub in the PWRGD path
while placing resistors RC115



CAD Note:
Trace width=12-15 mil, Spacing=20 mils
Max trace length= 500 mil

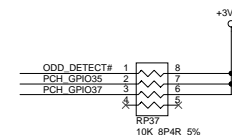
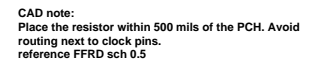
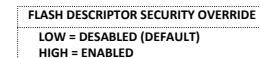


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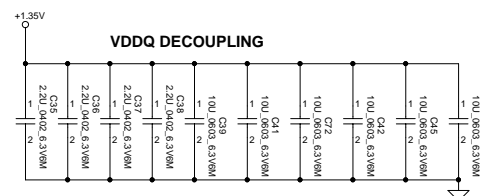
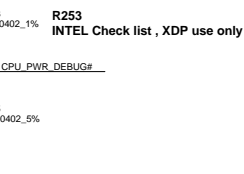
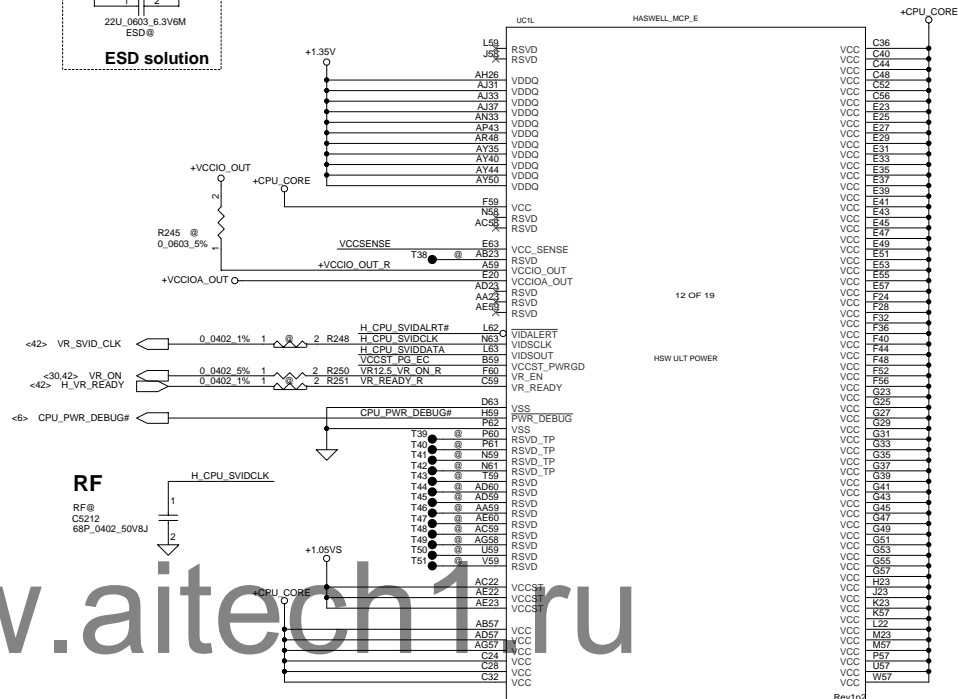
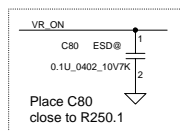
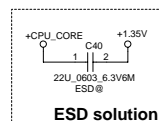


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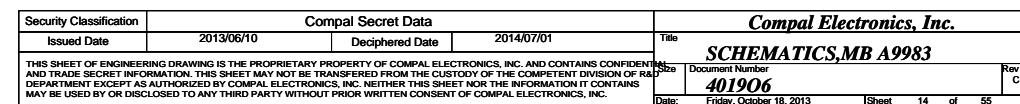
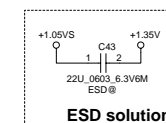
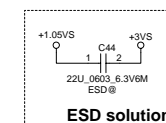
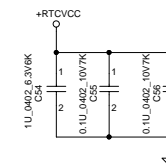
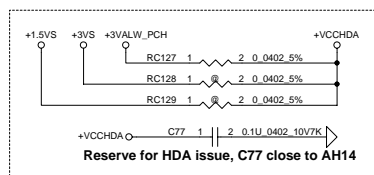


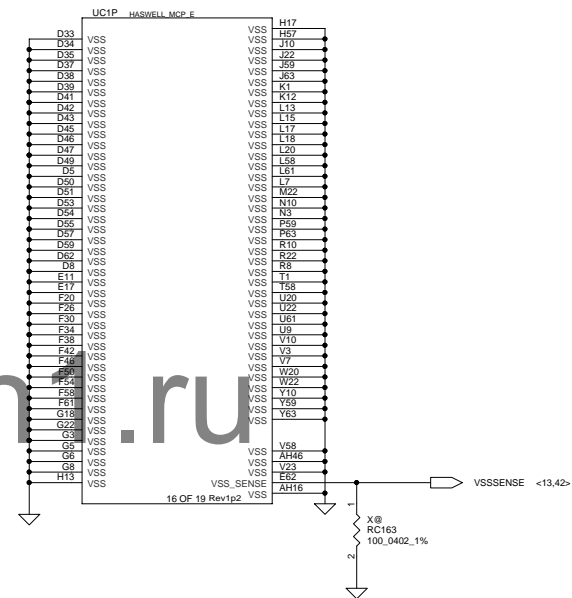
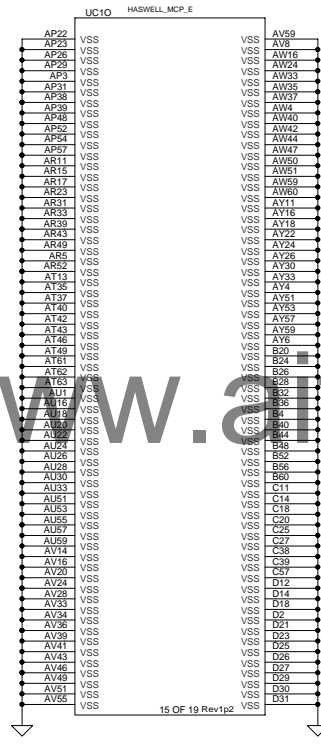
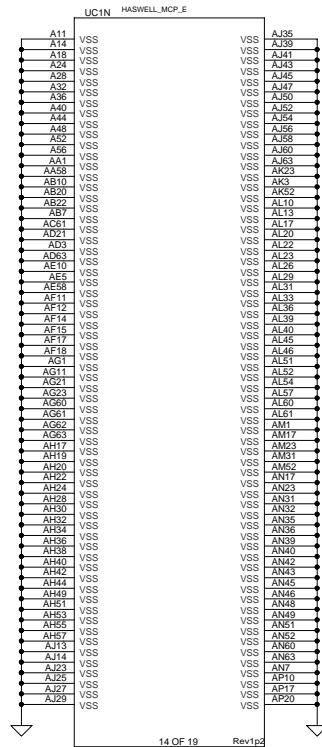
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**+1.35V : 470UF/2V/7343 *2 (PWR)
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4**

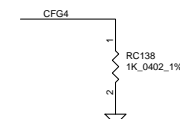
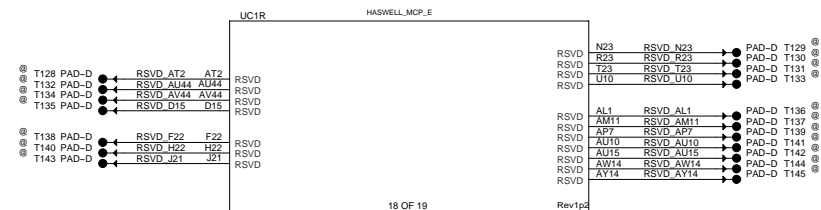
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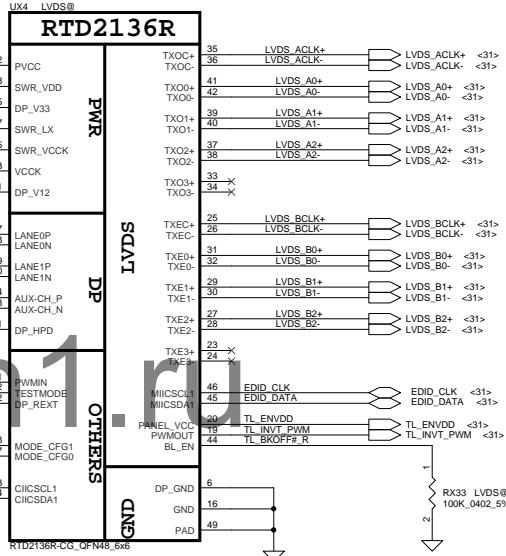
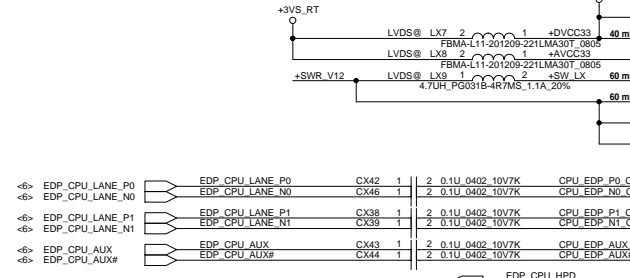
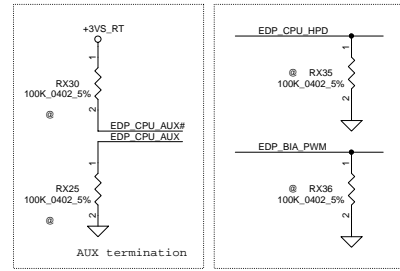
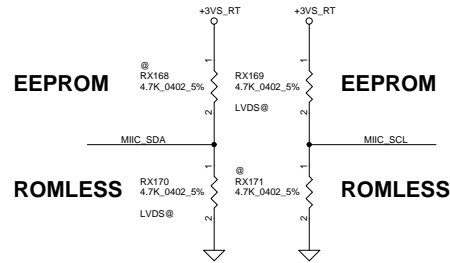
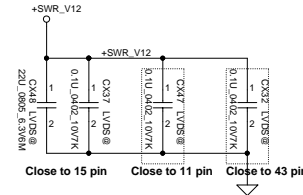
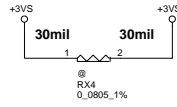
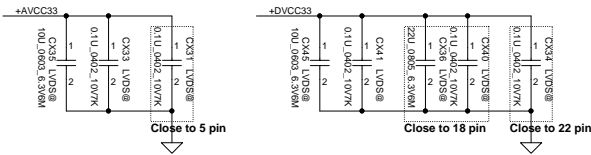
CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU

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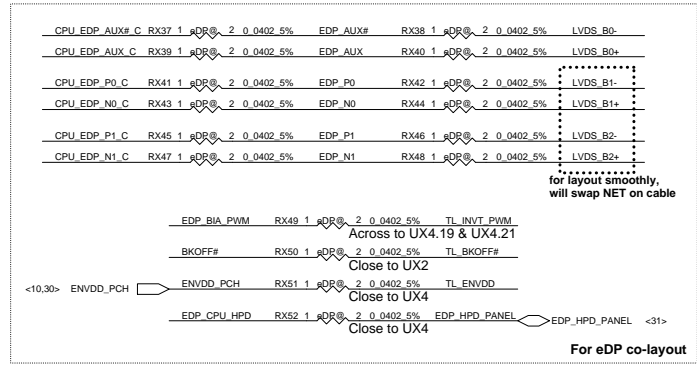
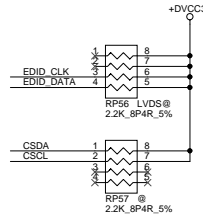
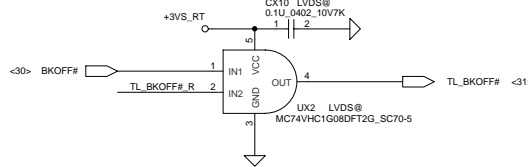
Display Port Presence Strap	
CFG4	<p>1: Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0: Enabled; An external Display Port device is connected to the Embedded Display Port</p>

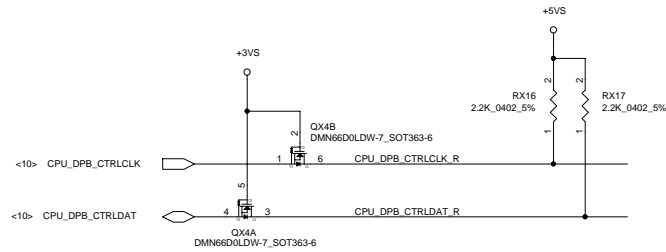
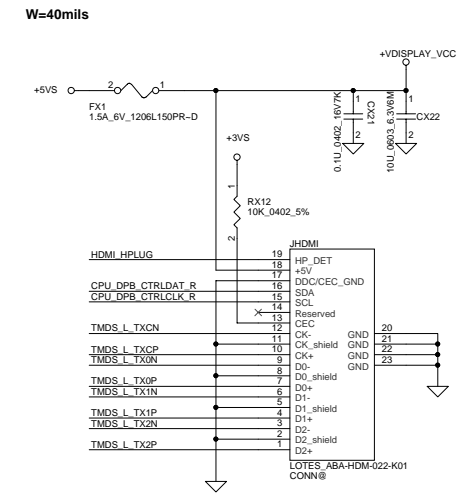
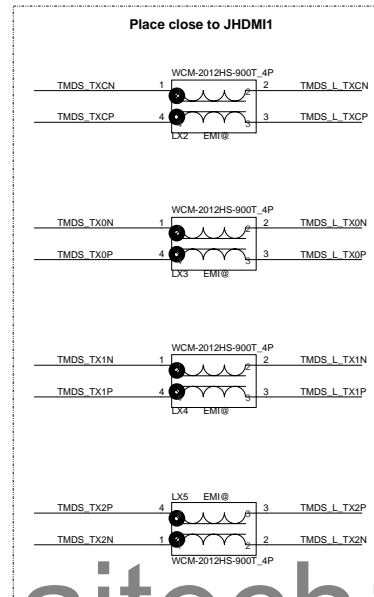
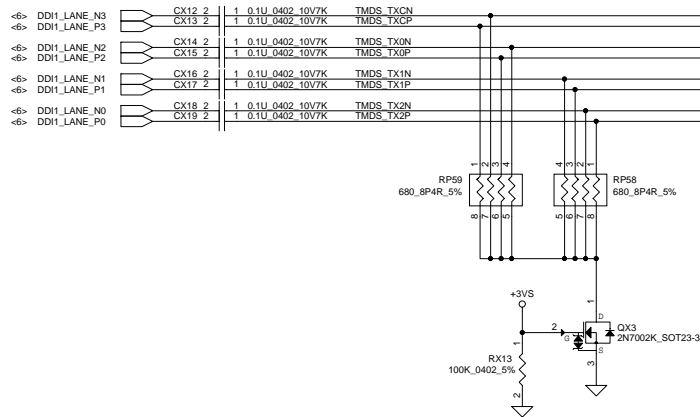
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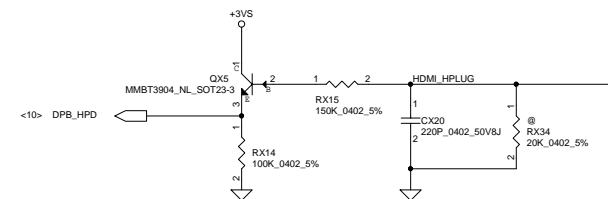
RTD2136S : SA00004NW10
RTD2136R : SA000067100

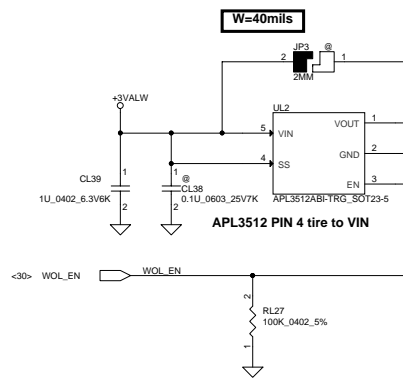
Vendor advise reserve it





TMD5_L_TXCN	@EMI@	CX23	1	2	3.3P_0402_50V8C
TMD5_L_TXCP	@EMI@	CX24	1	2	3.3P_0402_50V8C
TMD5_L_TX0N	@EMI@	CX25	1	2	3.3P_0402_50V8C
TMD5_L_TX0P	@EMI@	CX26	1	2	3.3P_0402_50V8C
TMD5_L_TX1N	@EMI@	CX27	1	2	3.3P_0402_50V8C
TMD5_L_TX1P	@EMI@	CX28	1	2	3.3P_0402_50V8C
TMD5_L_TX2N	@EMI@	CX29	1	2	3.3P_0402_50V8C
TMD5_L_TX2P	@EMI@	CX30	1	2	3.3P_0402_50V8C

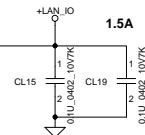




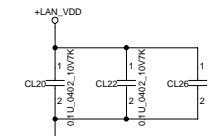
SS table

Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

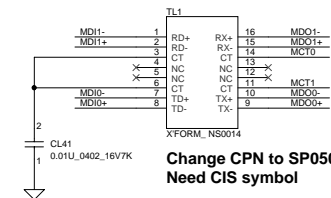
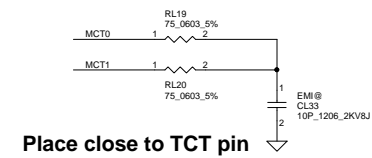
W=40mils +LAN_IO rising time : >1ms and <100ms



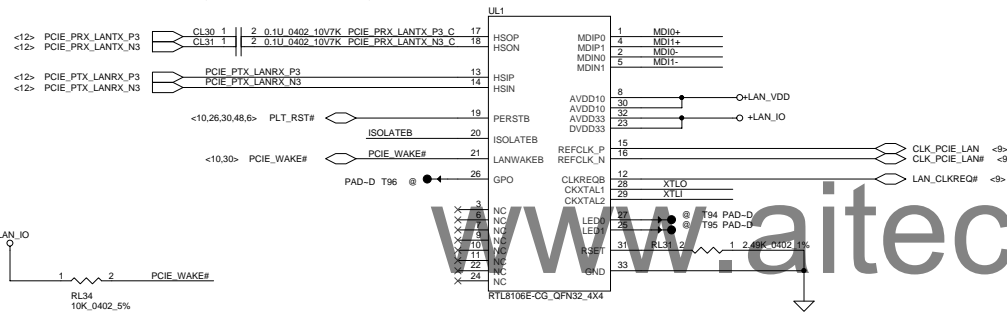
These caps close to Pin 23,32
For 8106E pop the capacitor close pin 23,32



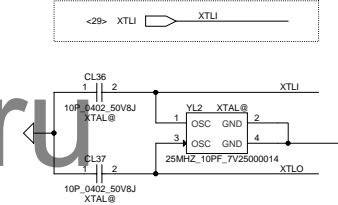
These caps close to Pin 8,30
For 8106E pop capacitor close to pin 8,30



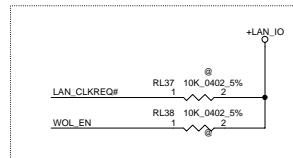
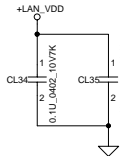
CL30, CL31 close to UL1 Pin 17, 18



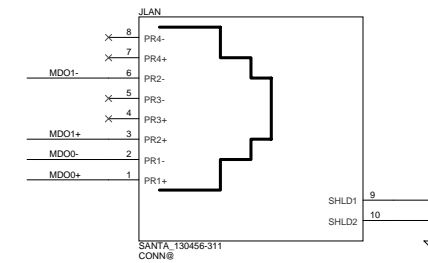
For GCLK



W=20mils

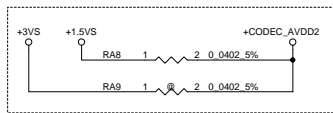


Reserve 10K pull LAN_IO

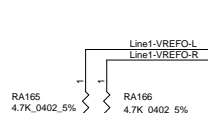


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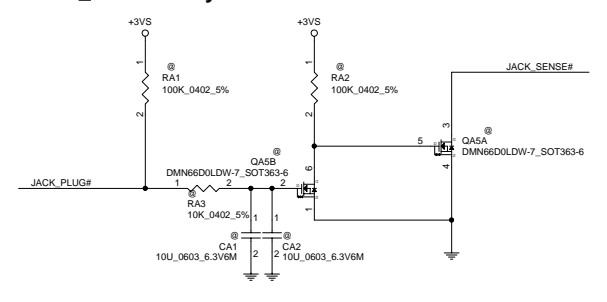
Reserve for HDA issue



Reserve for HDA issue

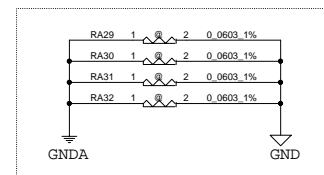


JACK_PLUG Delay circuitis



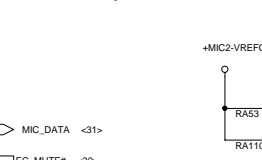
Reserve for cancel Delay circuitis

JACK_PLUG# RA4 1 2 0.0402 1% JACK_SENSE#

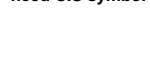


Place on the moat between GND & GNDA.

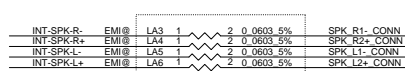
RA51, RA33 place close to UA1



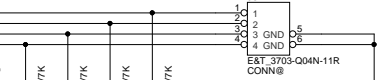
SM01000BV00 need CIS symbol



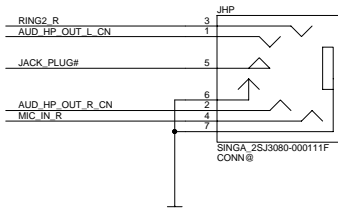
Close to UA1
Pin11,13,14,16



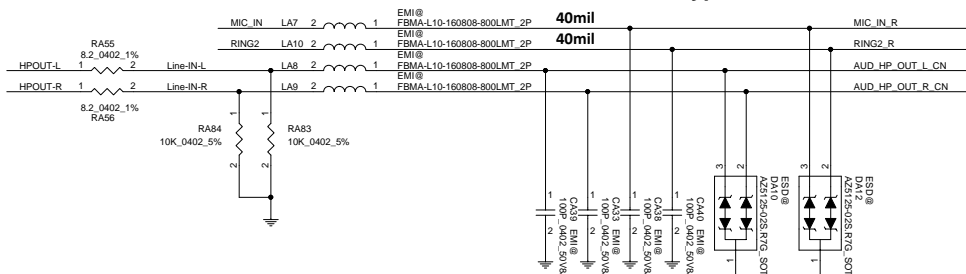
close to Codec



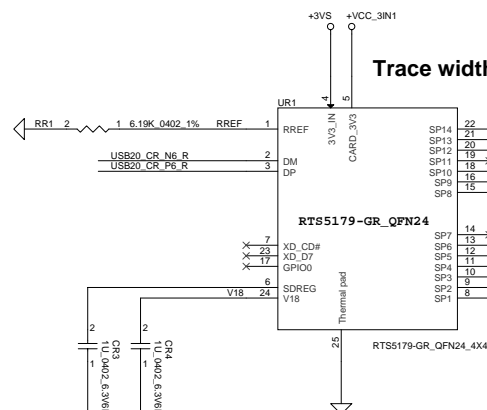
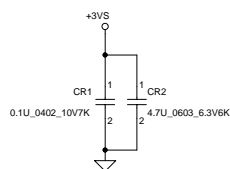
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil



iPhone and Nokia type Combo Jack



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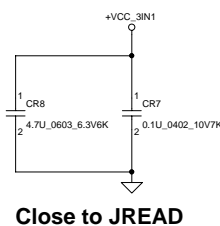
For EMI request. Place close to UR1

Timing diagram showing two signals: MS_D2_SD_CLK and MS_CLK_SD_WP. Both signals are represented by a square wave with a period of 100ns. The MS_D2_SD_CLK signal is labeled with 'EMI@ R2 22_0402_5%' and the MS_CLK_SD_WP signal is labeled with 'EMI@ R1 22_0402_5%'. The signals are shown with their respective pin connections: MS_D2_SD_CLK is connected to pin 1 of the EMI@ R2 component, and MS_CLK_SD_WP is connected to pin 1 of the EMI@ R1 component. The signals are also connected to the MS_D2_SD_CLK and MS_CLK_SD_WP pins of the chip, which are labeled with 'MS_D2_SD_CLK' and 'MS_CLK_SD_WP' respectively. The signals are shown with their respective pin connections: MS_D2_SD_CLK is connected to pin 1 of the EMI@ R2 component, and MS_CLK_SD_WP is connected to pin 1 of the EMI@ R1 component. The signals are also connected to the MS_D2_SD_CLK and MS_CLK_SD_WP pins of the chip, which are labeled with 'MS_D2_SD_CLK' and 'MS_CLK_SD_WP' respectively.

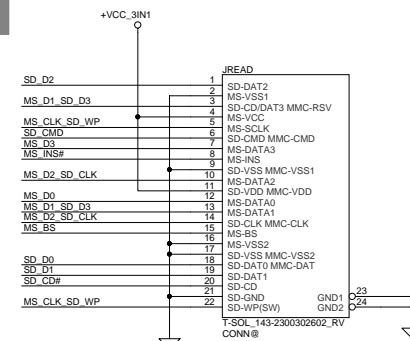
拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W

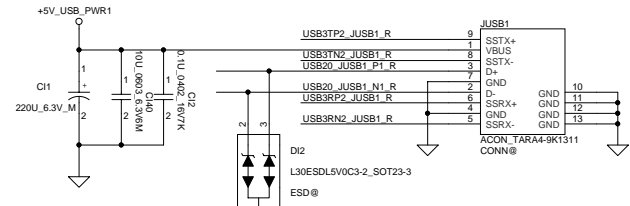
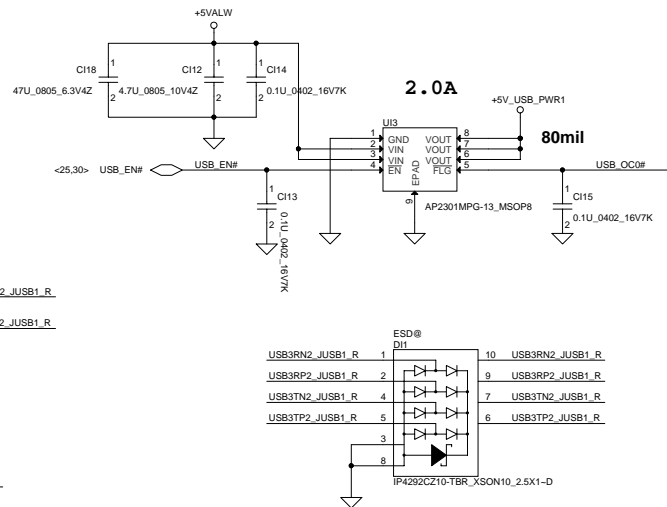
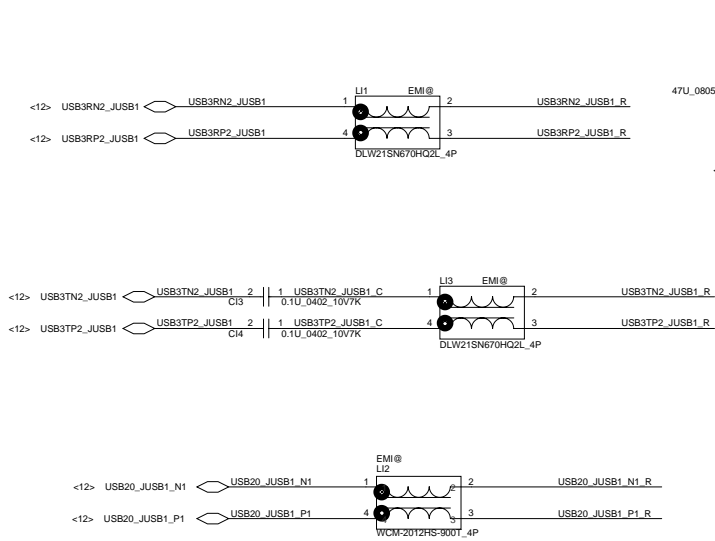
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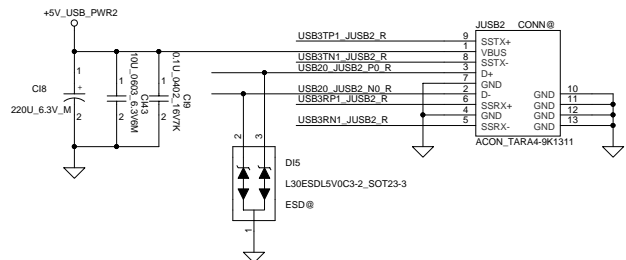
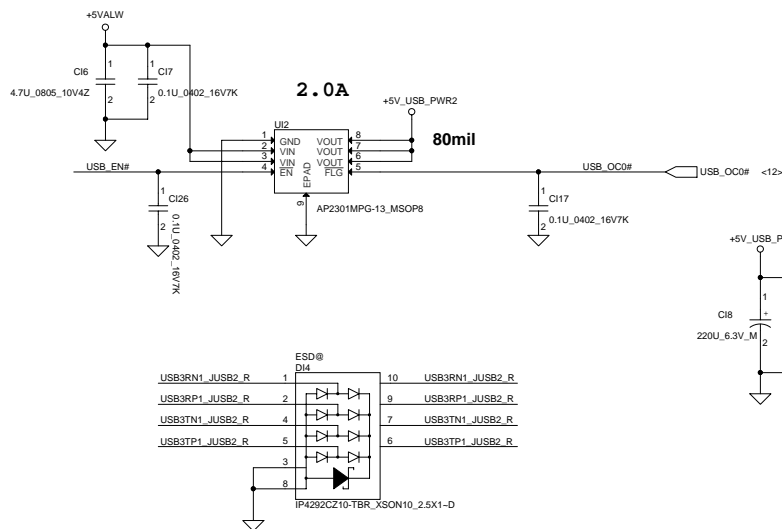
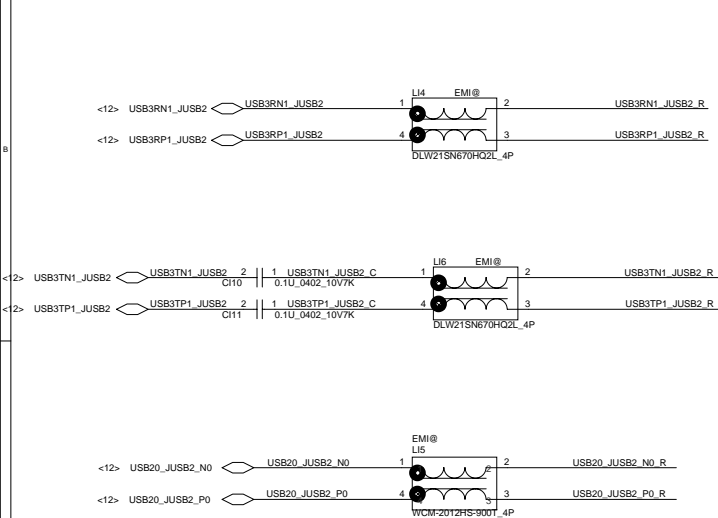
**For EMI request.
Place close to JREAD**



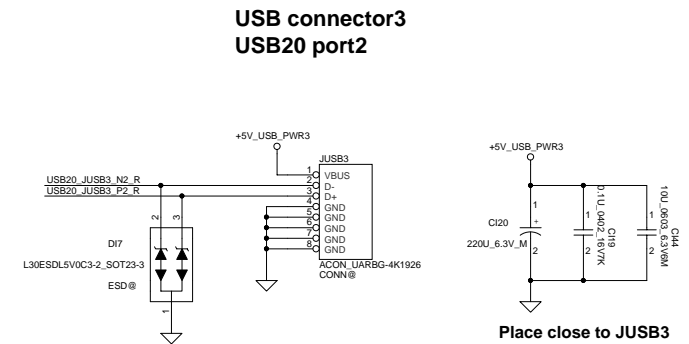
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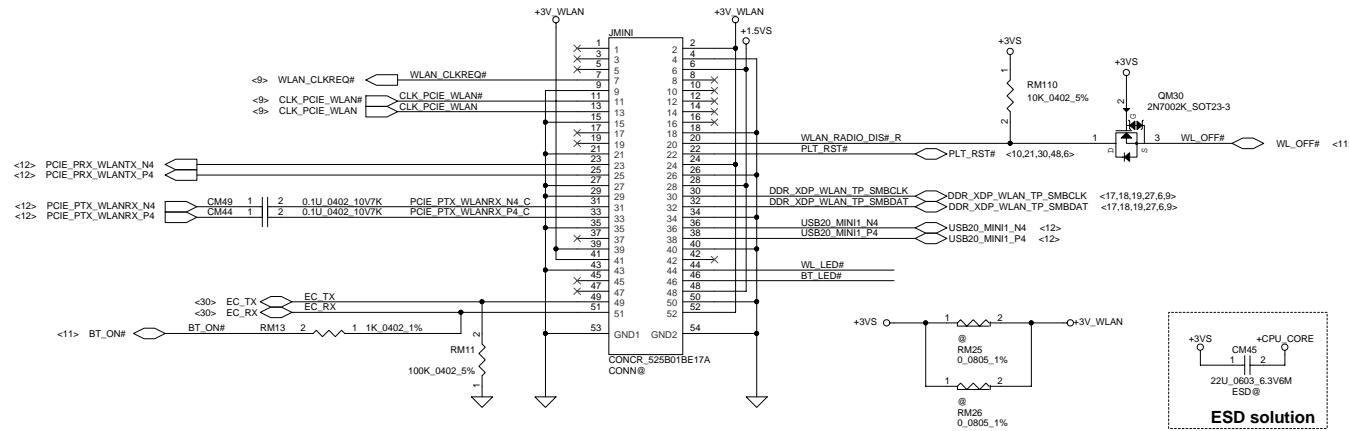
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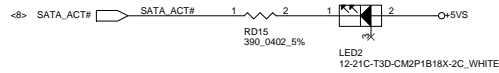
The schematic diagram illustrates the USB2.0 PHY circuit. It features a WCM-2012HS-900T 4P connector connected to the USB2.0 USBDB_P3 and USB2.0 USBDB_N3 signals. The circuit includes a 2.0A current source and various capacitors (CI21, CI31, CI30, CI25, CI32) for filtering and timing. The USB2.0 PHY chip (AP2301MPG-13_MS08) is the central component, with its pins connected to the USB signals and power. The output of the PHY is connected to a USB connector4 USB20 port3.

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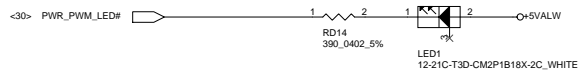
Mini WLAN/WIMAX H=6.7



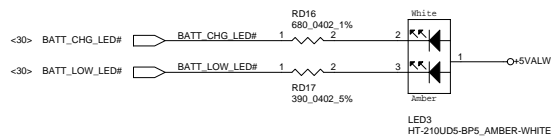
HDD LED



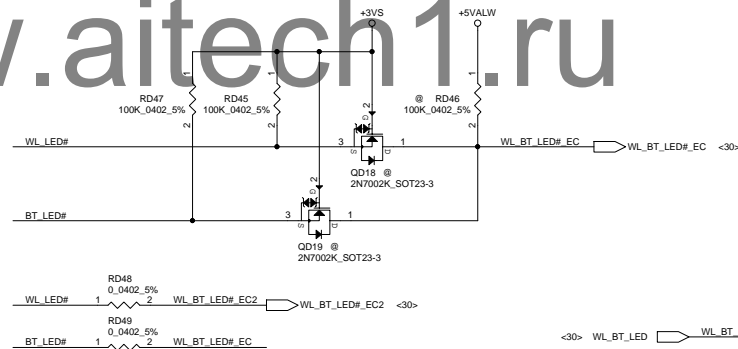
Power LED



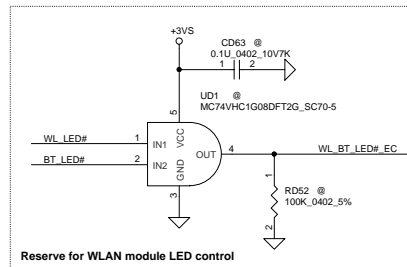
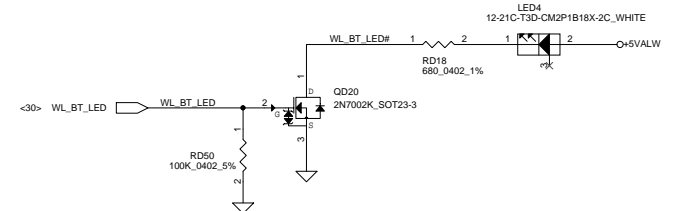
Battery LED



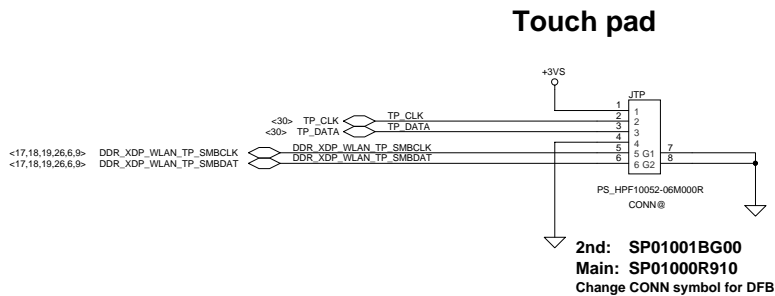
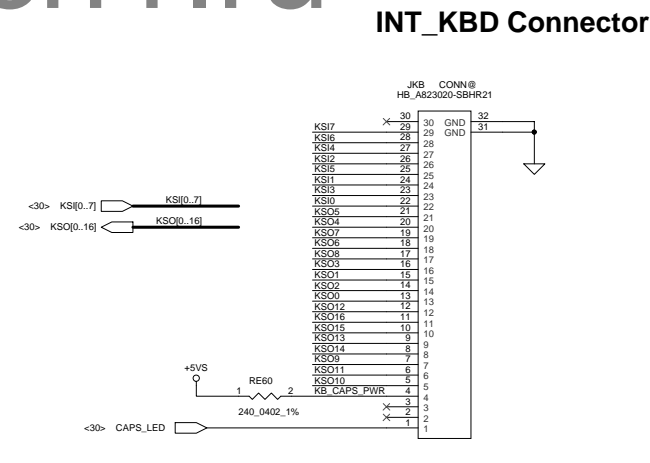
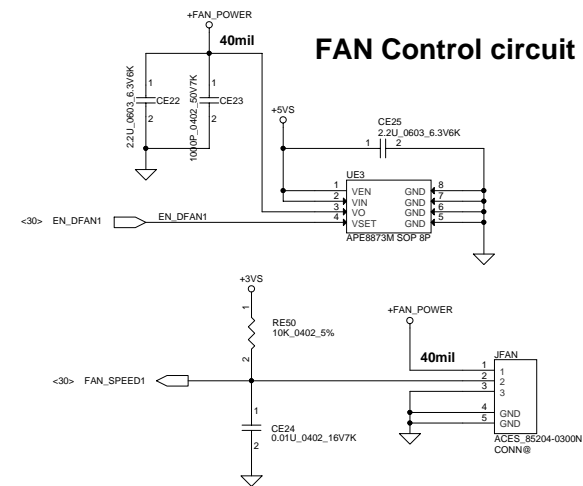
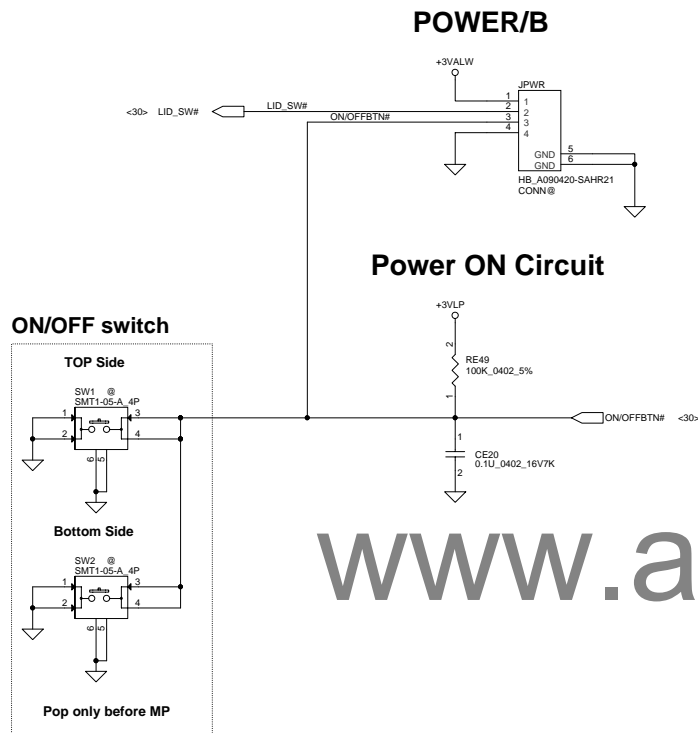
10mils, All pins



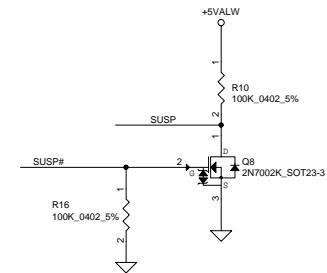
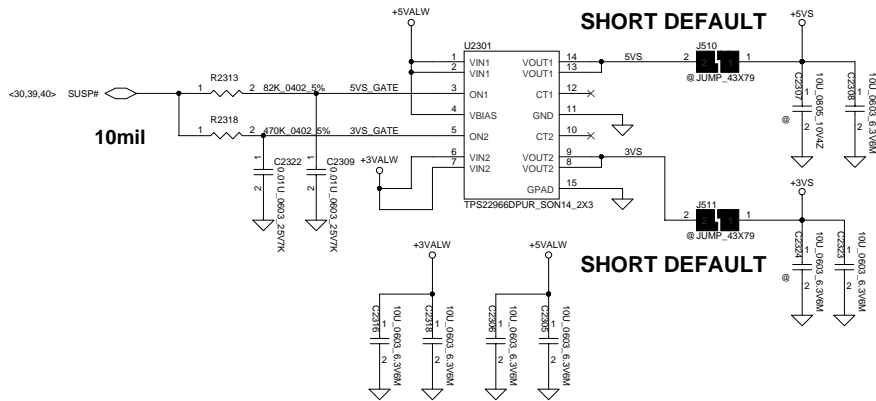
Wireless LED



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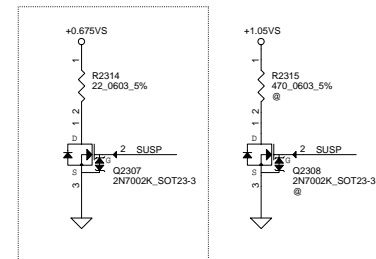
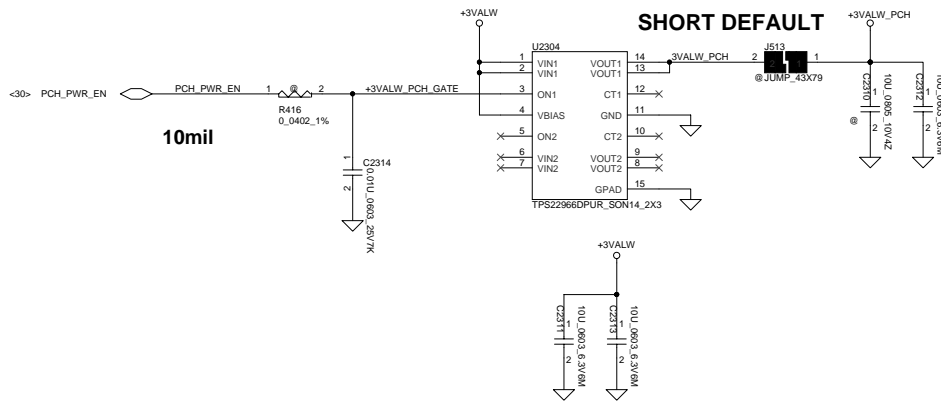


+5VS and +3VS switch



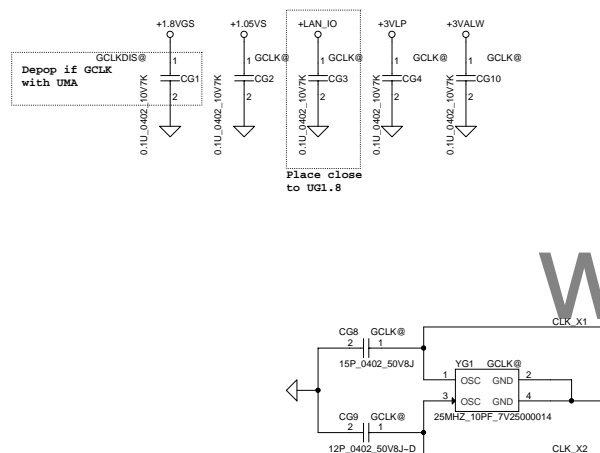
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+3VALW_PCH switch



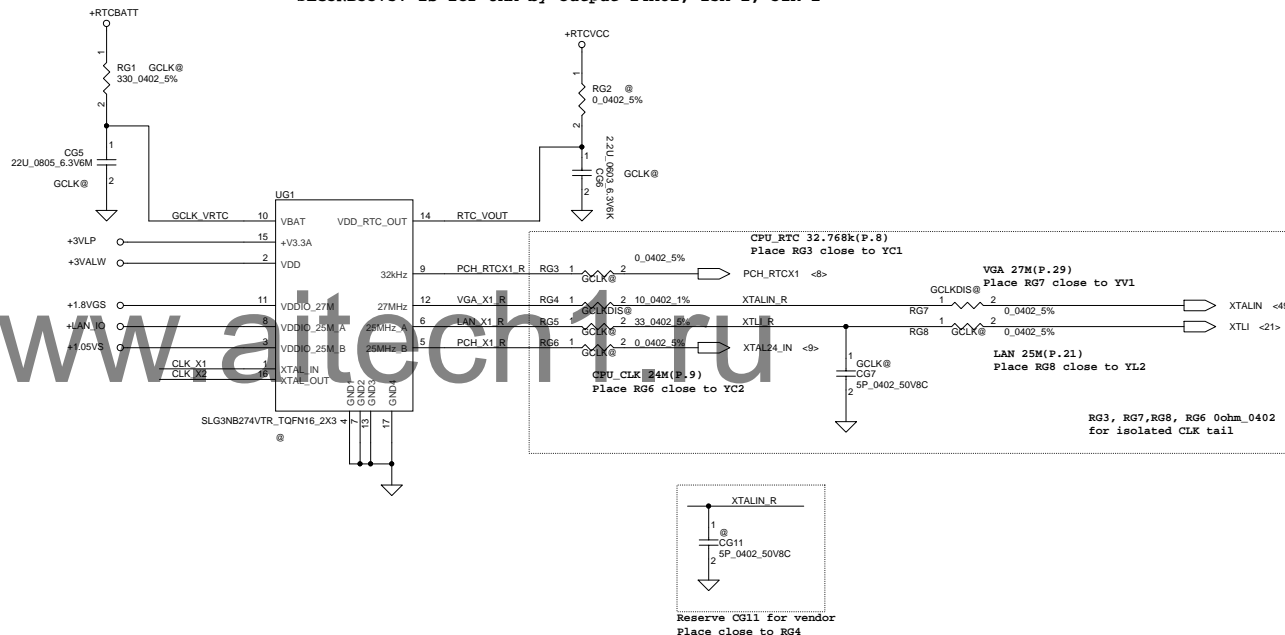
For Intel S3 Power Reduction

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UG1 GCLKUMA@
UG2 GCLKDIS@
SLG3NB244VTR TQFN 16P CLK GEN SLG3NB244VTR TQFN 16P CLK GEN

SLG3NB3374V is for DIS by output 24M*1,25M*1, 27M*1, 32K*1
SLG3NB3375V is for UMA by output 24M81, 25M*1, 32K*1



PLT_RST#
CE36 ESD@
0.047U_0402_16V4Z
Place CC30
close to RC51.1

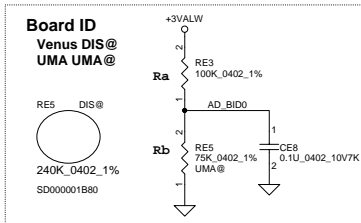
+3VALW
RE7 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161 162 163 164 165 166 167 168 169 170 171 172 173 174 175 176 177 178 179 180 181 182 183 184 185 186 187 188 189 190 191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 256 257 258 259 260 261 262 263 264 265 266 267 268 269 270 271 272 273 274 275 276 277 278 279 280 281 282 283 284 285 286 287 288 289 290 291 292 293 294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329 330 331 332 333 334 335 336 337 338 339 340 341 342 343 344 345 346 347 348 349 350 351 352 353 354 355 356 357 358 359 360 361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389 390 391 392 393 394 395 396 397 398 399 400 401 402 403 404 405 406 407 408 409 410 411 412 413 414 415 416 417 418 419 420 421 422 423 424 425 426 427 428 429 430 431 432 433 434 435 436 437 438 439 440 441 442 443 444 445 446 447 448 449 450 451 452 453 454 455 456 457 458 459 460 461 462 463 464 465 466 467 468 469 470 471 472 473 474 475 476 477 478 479 480 481 482 483 484 485 486 487 488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504 505 506 507 508 509 510 511 512 513 514 515 516 517 518 519 520 521 522 523 524 525 526 527 528 529 530 531 532 533 534 535 536 537 538 539 540 541 542 543 544 545 546 547 548 549 550 551 552 553 554 555 556 557 558 559 560 561 562 563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587 588 589 590 591 592 593 594 595 596 597 598 599 600 601 602 603 604 605 606 607 608 609 610 611 612 613 614 615 616 617 618 619 620 621 622 623 624 625 626 627 628 629 630 631 632 633 634 635 636 637 638 639 640 641 642 643 644 645 646 647 648 649 650 651 652 653 654 655 656 657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675 676 677 678 679 680 681 682 683 684 685 686 687 688 689 690 691 692 693 694 695 696 697 698 699 700 701 702 703 704 705 706 707 708 709 710 711 712 713 714 715 716 717 718 719 720 721 722 723 724 725 726 727 728 729 730 731 732 733 734 735 736 737 738 739 740 741 742 743 744 745 746 747 748 749 750 751 752 753 754 755 756 757 758 759 760 761 762 763 764 765 766 767 768 769 770 771 772 773 774 775 776 777 778 779 780 781 782 783 784 785 786 787 788 789 790 791 792 793 794 795 796 797 798 799 800 801 802 803 804 805 806 807 808 809 810 811 812 813 814 815 816 817 818 819 820 821 822 823 824 825 826 827 828 829 830 831 832 833 834 835 836 837 838 839 840 841 842 843 844 845 846 847 848 849 850 851 852 853 854 855 856 857 858 859 860 861 862 863 864 865 866 867 868 869 870 871 872 873 874 875 876 877 878 879 880 881 882 883 884 885 886 887 888 889 890 891 892 893 894 895 896 897 898 899 900 901 902 903 904 905 906 907 908 909 910 911 912 913 914 915 916 917 918 919 920 921 922 923 924 925 926 927 928 929 930 931 932 933 934 935 936 937 938 939 940 941 942 943 944 945 946 947 948 949 950 951 952 953 954 955 956 957 958 959 960 961 962 963 964 965 966 967 968 969 970 971 972 973 974 975 976 977 978 979 980 981 982 983 984 985 986 987 988 989 990 991 992 993 994 995 996 997 998 999 1000

Reserve for ESD
CE27 ESD@
0.1U_0402_10V7K
CE28 ESD@
0.1U_0402_10V7K
Please close to EC

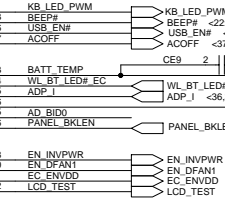
FAN_SPEED1
CE29
220P_0402_50V8J
Please close to EC

VR_HOT#
H_PROCHOT#
SN74LVC1G08DCR SC70-5
CE19
47P_0402_50V8J
Please close to EC

KB9012A3 change to
KB9012A4 SA000040B30

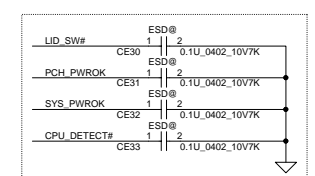
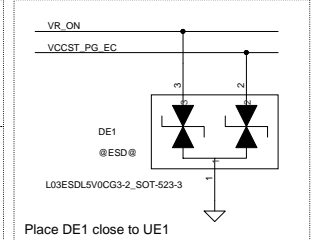


"KB_LED_PWM" for OAK 17 only



VR_ON
CE34 ESD@
0.1U_0402_10V7K
Place CE34
between DE1 and RE12

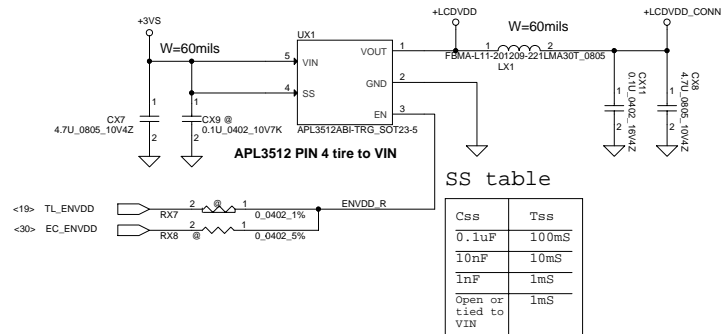
VCCST_PG_EC
CE35 ESD@
220P_0402_50V8J
Place CE35
between DE1 and UE1



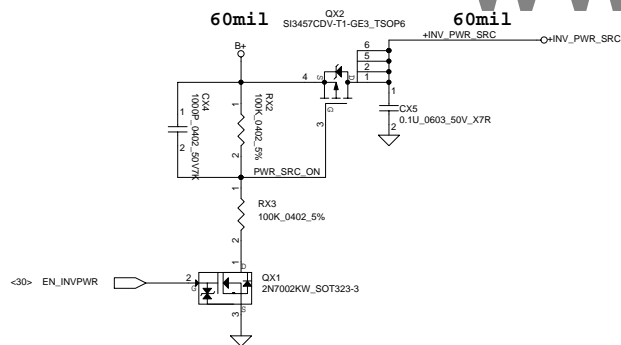
Place CE30,CE31,CE32,CE33 close to UE1

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2013/06/10		2014/07/01		Document Number	
2013/06/10		2014/07/01		401906	
2013/06/10		2014/07/01		Rev C	
2013/06/10		2014/07/01		Date: Friday, October 18, 2013	
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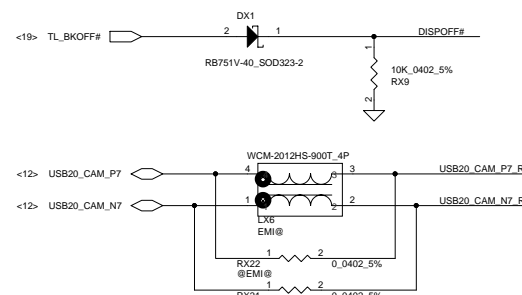
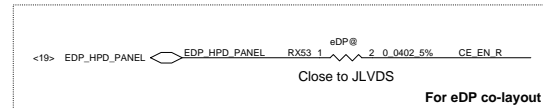
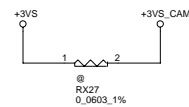
LCD PWR CTRL



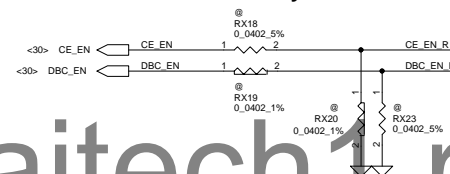
LCD backlight PWR CTRL



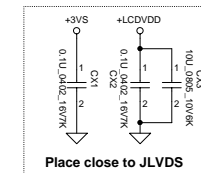
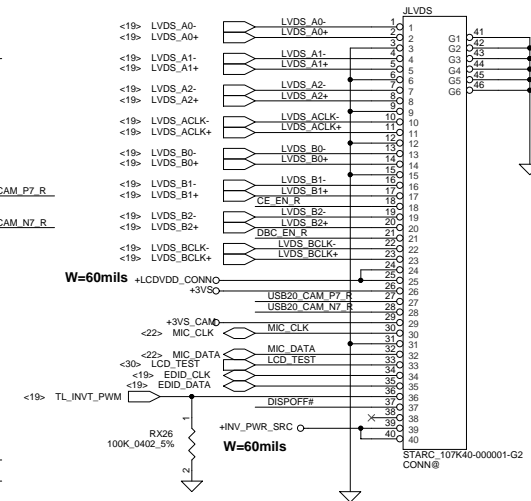
Webcam PWR CTRL



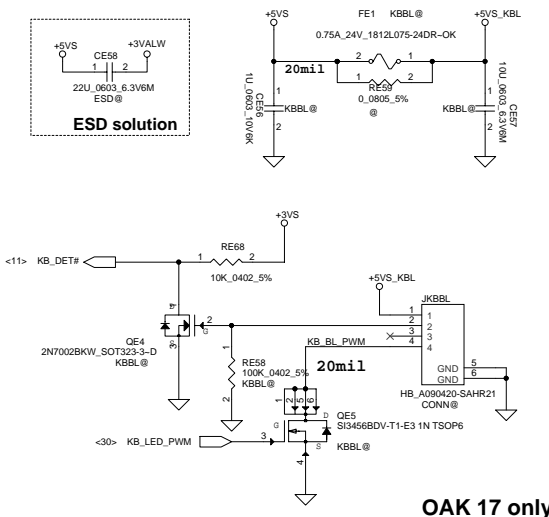
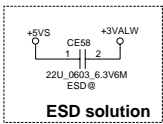
CE_EN_R only for reserve.



LVDS Connector

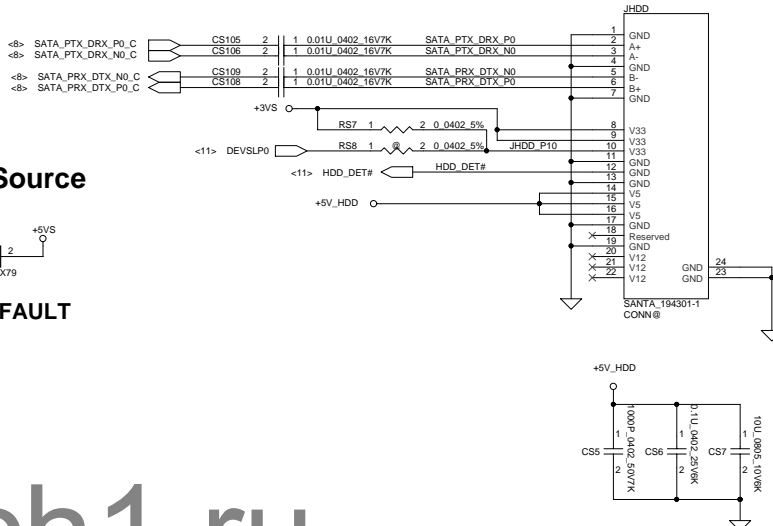


* Key Board Back Light

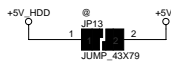


OAK 17 only

SATA HDD Connector

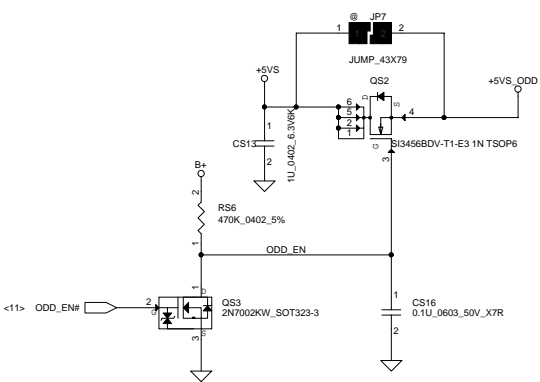


+5V_HDD Source

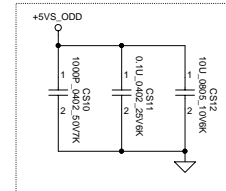
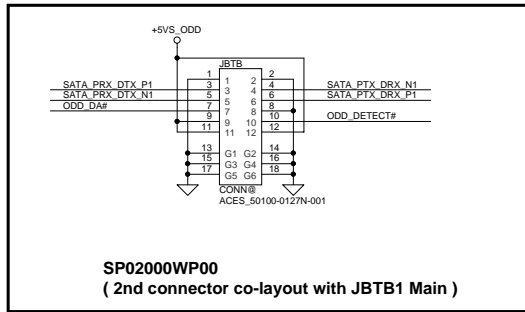
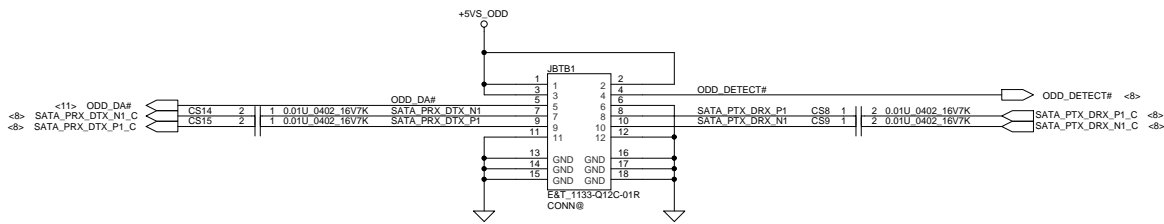


SHORT DEFAULT

ODD Power Control

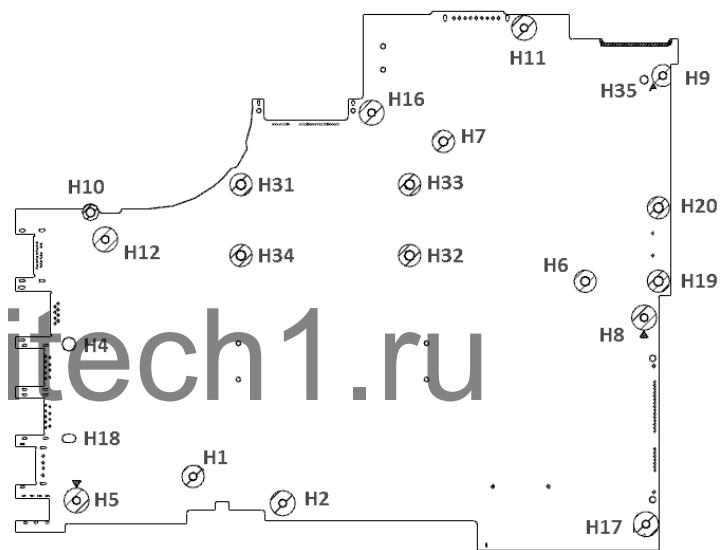
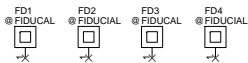
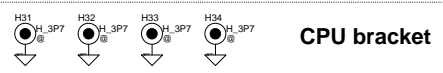
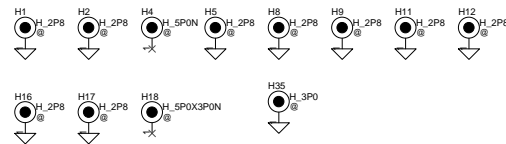


ODD BTB Connector



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Screw Hole



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				Rev	C

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2							
3							
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www.aitech1.ru

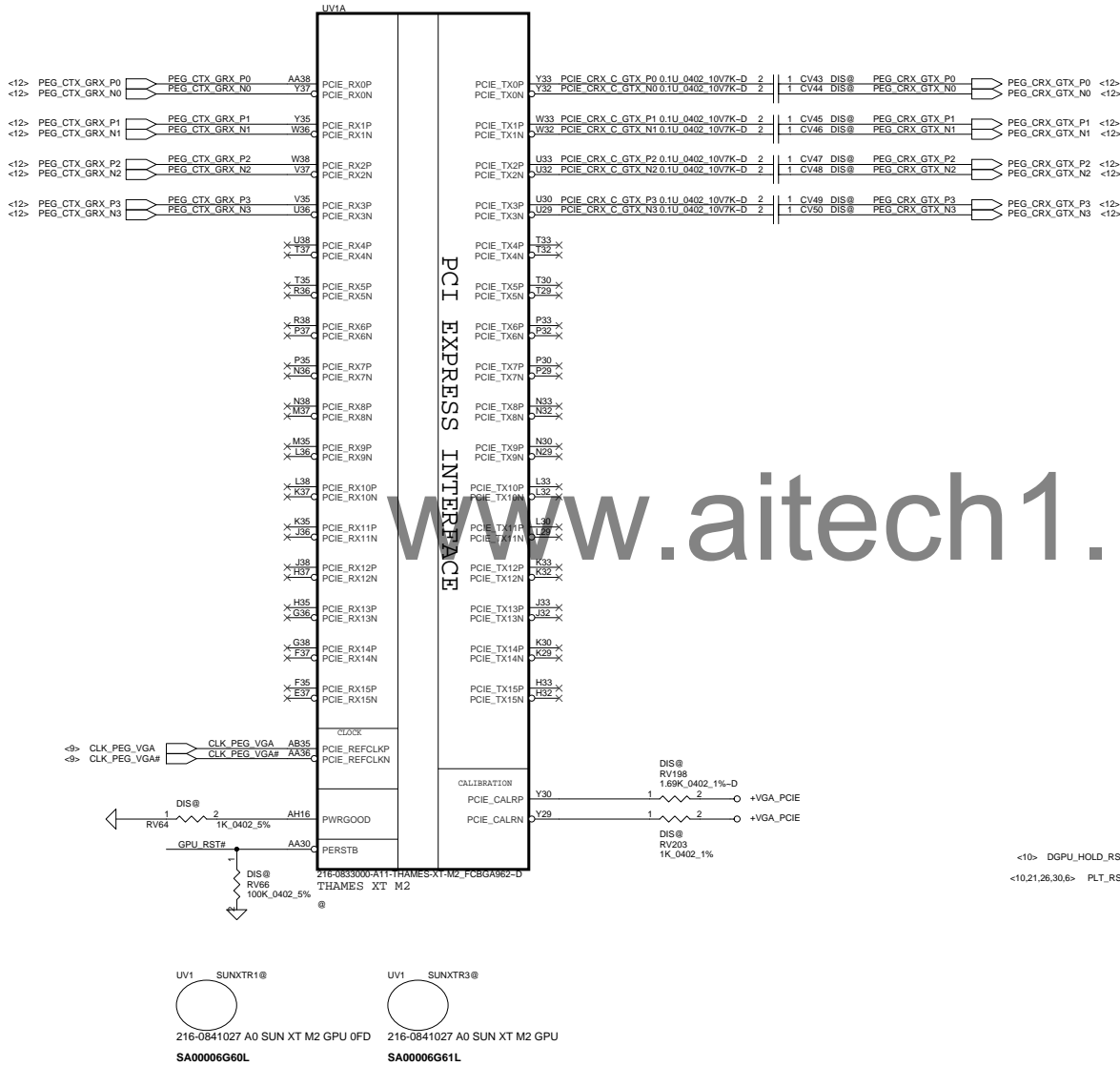
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40							
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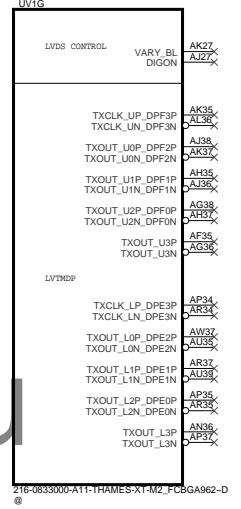
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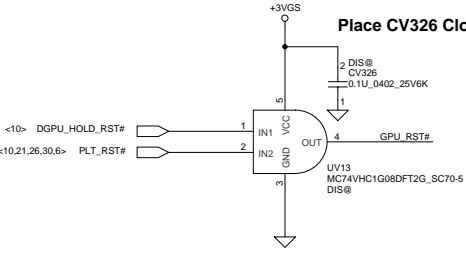
GFX PCIE LANE REVERSAL



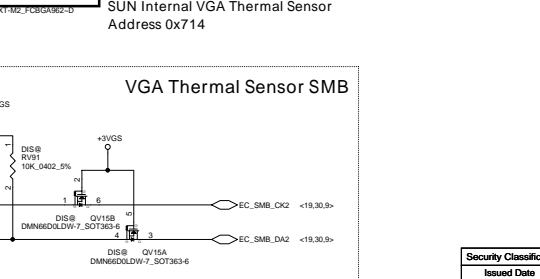
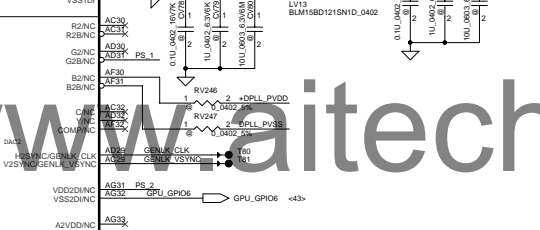
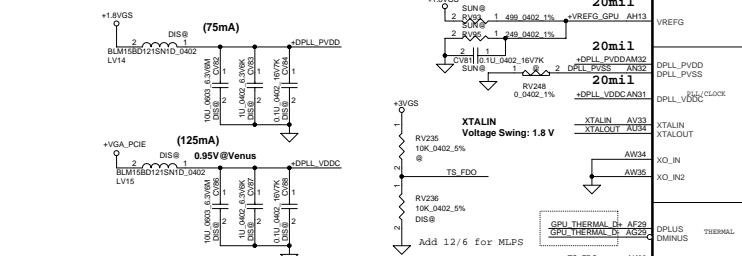
LVDS Interface





Place CV326 Close to UV13



GPIO1	GPU_GPIO1
GPIO2	GPU_GPIO2
GPIO7	N.C
GPIO11	GPU_GPIO11
GPIO12	GPU_GPIO12
GPIO13	GPU_GPIO13
GPIO14	N.C
GPIO18	N.C



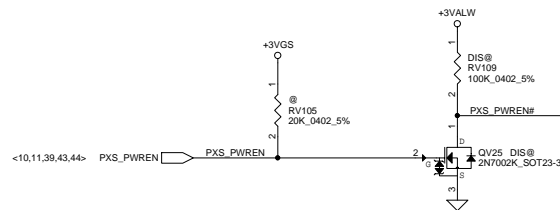
 TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output saving for mobile mode 1: full Tx output saving (Default setting for Desktop)
	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)
 TX_DEEMP_EN		

	Vendor	RV241	RV242	Bits [3:1]
★ 128MX16 (10B) DDR3	HYUNDAI Hynix 2Gb SA00000EH40L(R1) SA00000EH41L(R3)	NC	4.75K	000
128MX16 (10B) DDR3	SAMSUNG Samsung 2Gb SA000005SH0L(R1) SA000005SH1L(R3)	8.45K	2K	001
128MX16 (10B) DDR3	MICRON Micron 2Gb SA000005XB0L(R1) SA000005XB1L(R3)	4.75K	NC	111

PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails except VDDR3,PCIE_VDDC and 1.8V rail

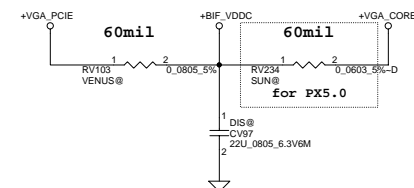
Note:

PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF



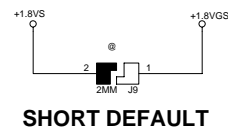
for PX4.0 and PX5.0

Switch circuits in BACO desings for Thames/Seymour only
55mA@1.0V, in BACO mode



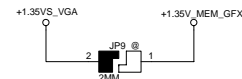
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+1.8VS TO +1.8VGS



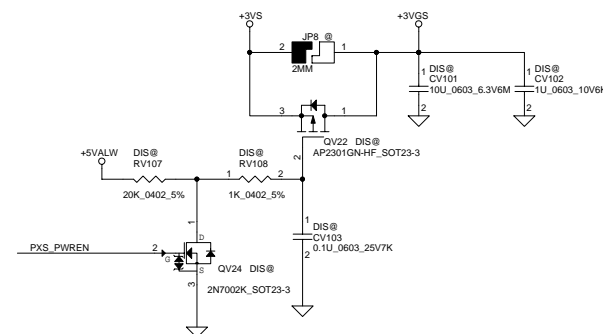
SHORT DEFAULT

+1.35VS_VGA TO +1.35V_MEM_GFX

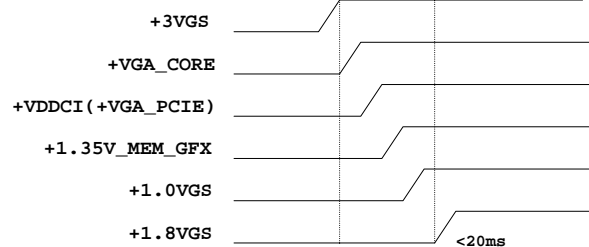


SHORT DEFAULT

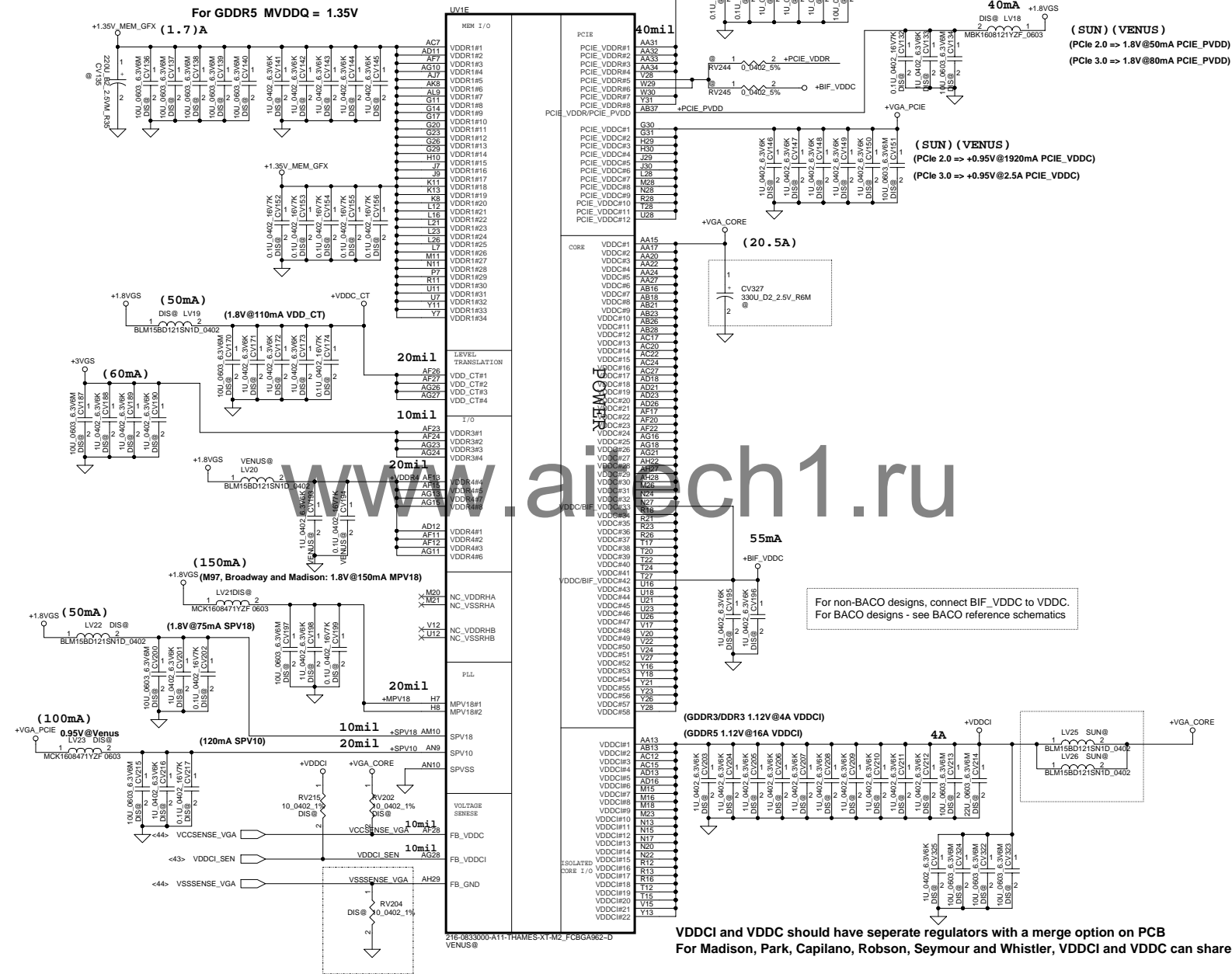
+3VS TO +3VGS



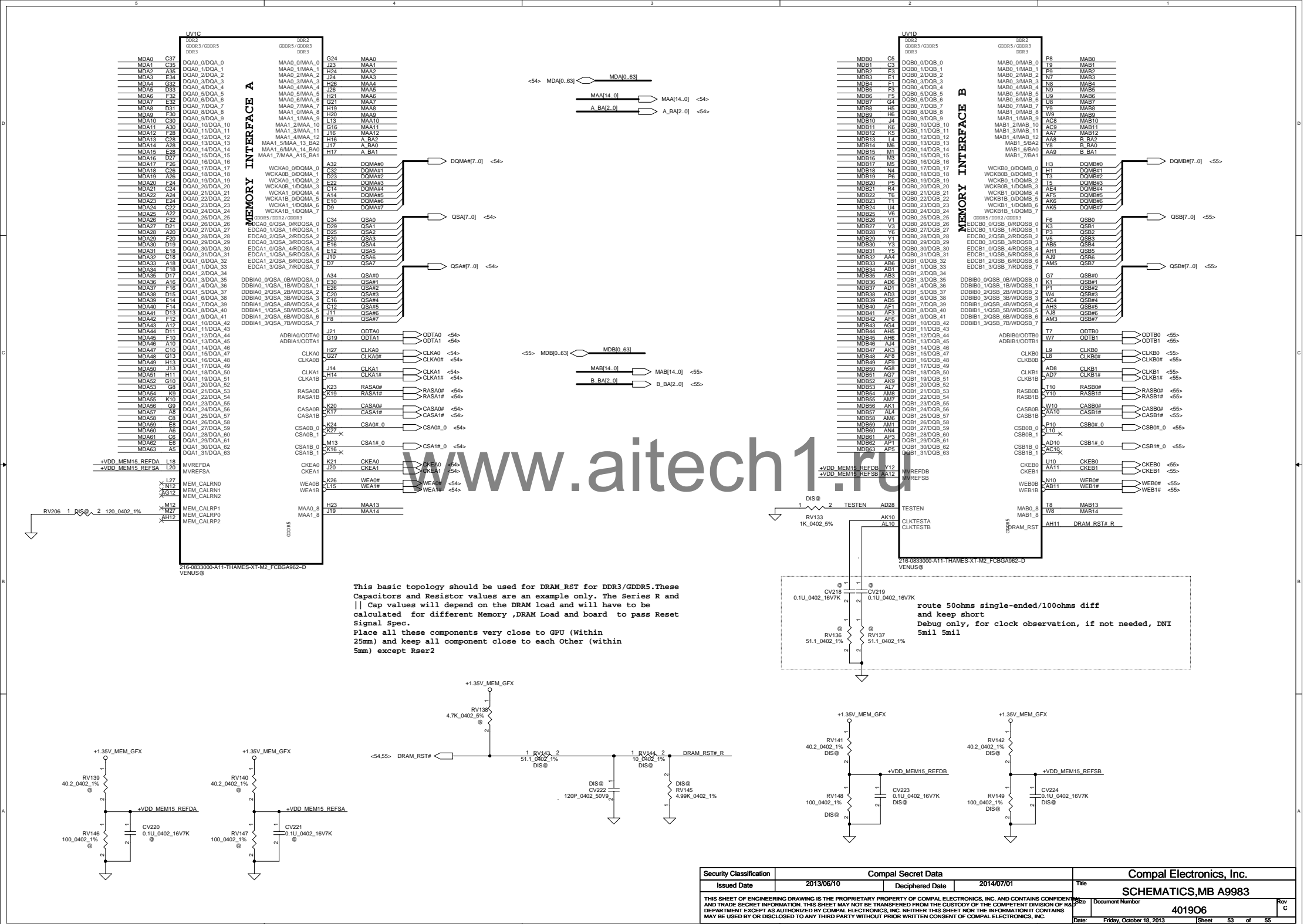
Power sequence of Sun XT,Venus Pro,Venus XT



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Channel A: 256MB DDR3

UV18 @

UV19 @

UV20 @

UV21 @

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Channel A: 256MB DDR3

UV18 @

UV19 @

UV20 @

UV21 @

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Issued Date: 2013/06/10

Deciphered Date: 2014/07/01

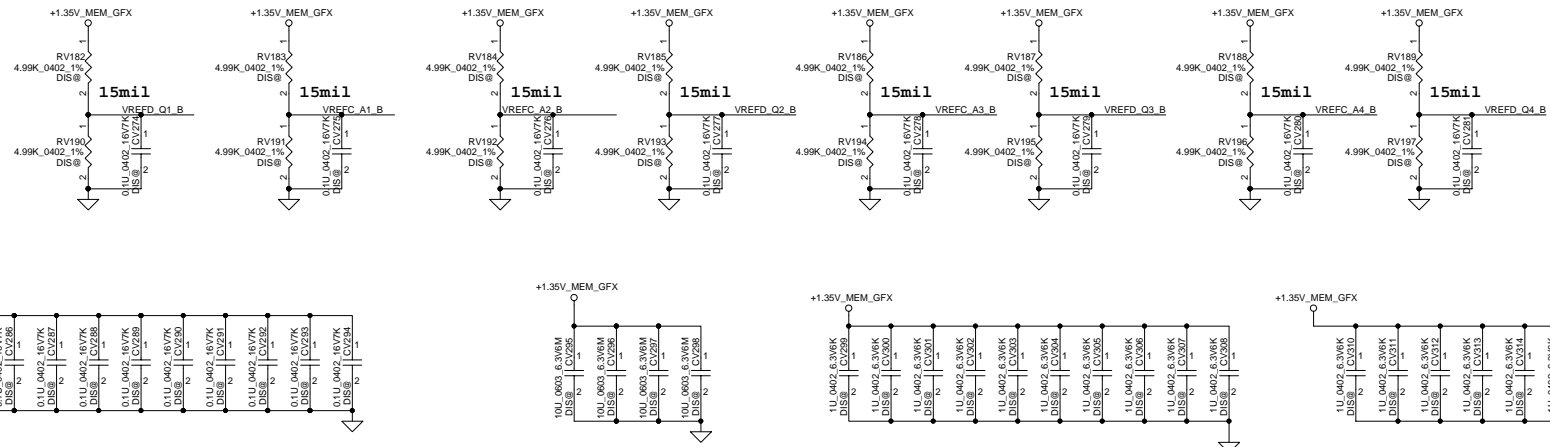
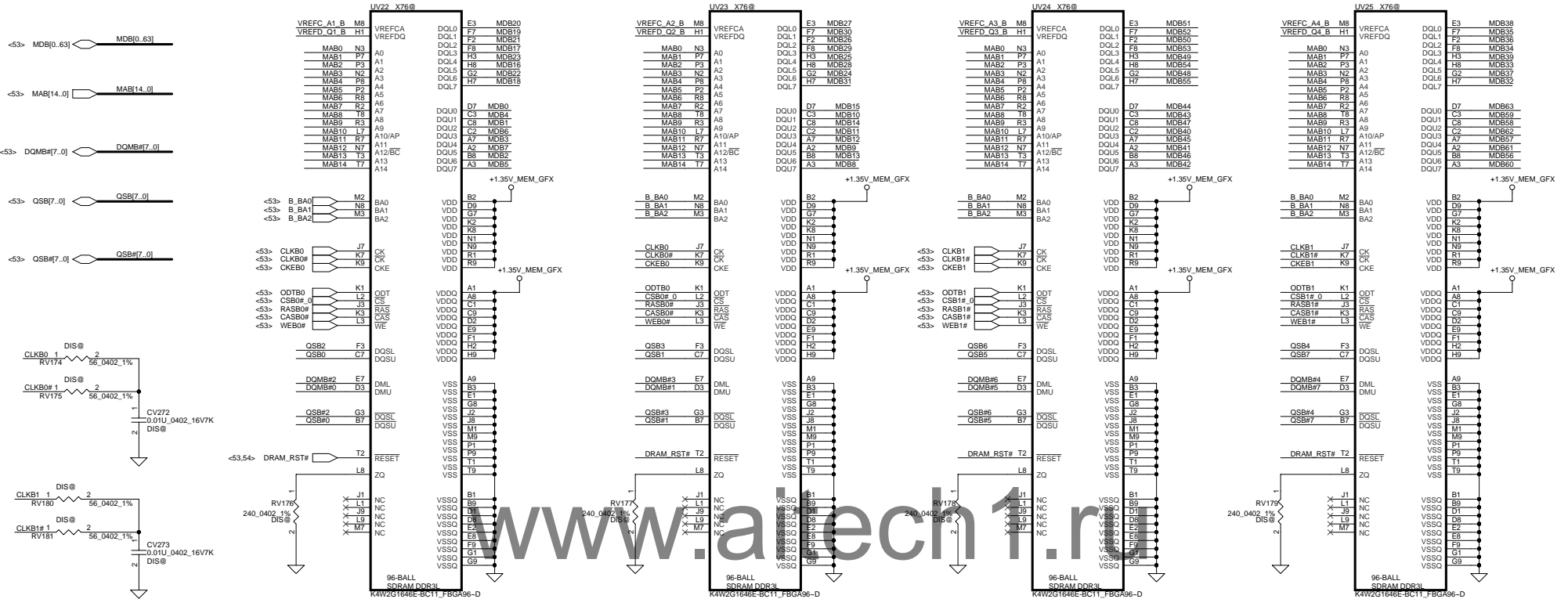
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CHANNEL B: 256MB DDR3



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